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Self-Repairable Multiplexer in Real Time for Fault Tolerant Systems

Dr. G C Manjunatha , Kiran P V , Venumadhava M

Assoc. Prof , Asst. Professor, Asst. Professor

gc.manjunatha@gmail.com , pv.kiran1977@gmail.com , venudsp@gmail.com

Department of ECE, Proudhadevaraya Institute of Technology, Abheraj Baldota Rd, Indiranagar,

Hosapete, Karnataka-583225

***Abstract*— Very large scale integration allows for a greater density of transistors on a single chip. A system or chip becomes increasingly prone to errors as the distance between circuits or transistors decreases. To prevent erroneous findings, fault tolerant mechanisms must be in place. A multiplexer is a piece of equipment that uses a select signal to choose which input signals to use. All of the previous research has focused on self-checking multiplexers. A self-repairing 2:1 multiplexer capable of fixing both temporary and permanent errors is suggested in this study. The self-repairing multiplexer is suggested in two distinct architectural forms. To fix the multiplexer issue, the first design incorporates extra circuitry. Multiplexer components, such as OR and AND gates, are self-repairing in the second design. These multiplexer designs are capable of detecting and fixing both single and multiple problems on their own. All errors are fully recovered by the suggested designs. The functioning of the circuits is confirmed by simulation using the Cadence program.**

***Index Terms*— VLSI, Fault, Error, Self checking, Self repairing.**

I. INTRODUCTION

As the technology is scaling down, chip density is increasing so that millions of transistors are embedded on a single die. The yield may decrease due to process
variations, deviation in parameters and lithographic effects [13]. This advanced microelectronic technologies more susceptible to faults [4].

The response of a circuit may be invalid because of presence of faults [5-8]. This leads to inaccurate results. Fault secure systems are very much needed to withstand faults [910]. So the self checking and repairing is necessary for correct operation of the circuit. In self checking the fault is detected by circuit itself and in self repairing the circuit can repair itself and produces correct output [11]. The overall circuit performance depends on individual gates of the circuit. Using small number of gates for design can increase the performance in terms of delay, area and power.

To get high speed the critical path should be as minimum as possible. Similarly to get low power less number of gates are used at circuit level without compromising the accuracy of the circuit [12-14]. Multiplexers are used in wide variety of applications like adders, multipliers, communication, digital signal processing etc. [15-19] Based on the selection signal multiplexer will select the input data and passes it to the output. The presence of fault in a multiplexer causes invalid data at the output. The multiplexer should be fault secure so that it gives valid data at the output even though faults are present in it. The paper is organized as follows. The self checking multiplexer described in section II, Proposed layout of the self repairing multiplexer 1 and 2 are explained in section III and IV. The layout and equivalent circuit simulation results are discussed in section V. Finally conclusion is given in section VI.

II. SELFCHECKINGMULTIPLEXER

Self checking multiplexer was proposed in [6]. This self checking multiplexer designed by using four transmission gates and an inverter as shown in Fig. 1. When CS is low S0N is passed to SN. Similarly when CS is high S1N is passed to SN. Thus it implements the function of multiplexer. In this self checking multiplexer when SN and SN_bar are same then it shows the presence of a fault. By using this structure only fault is detected and can't be repairable. To make the multiplexer self repairing two different structures are

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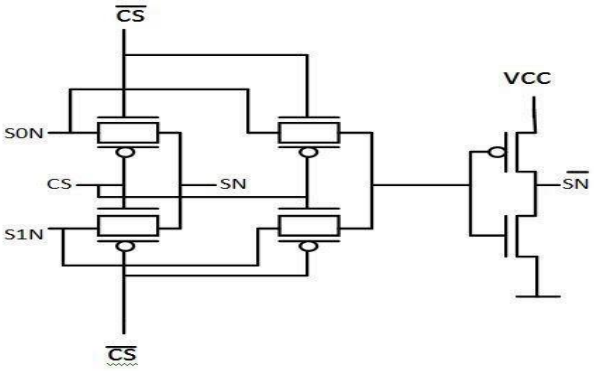

proposed. The CS bar signal is the inverted signal of CS. Fig. 1. Self checking multiplexer [6].

III. PROPOSED SELF REPAIRING MULTIPLEXER 1

This section describes the proposed self repairing multiplexer1 which uses additional circuitry to detect and repair fault. The circuit diagram is shown in Fig. 2.

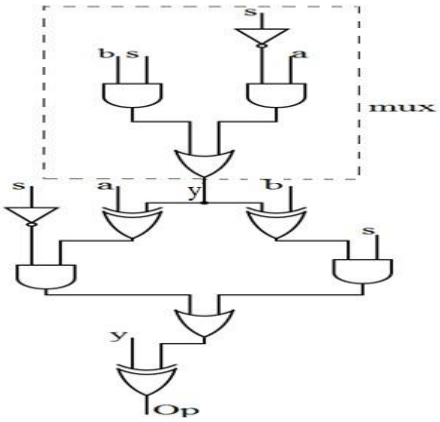

Fig. 2. Proposed self repairing multiplexer 1

In Fig. 2 the circuit enclosed in square box shows the basic structure of 2:1 multiplexer. Remaining structure which is not included in the square box is used for repairing the above 2:1 multiplexer. The circuit is able to detect all possible single and multiple faults present in the 2:1 multiplexer and repairs the circuit. The circuit gives 100% error recovery.

Consider Fig. 2. Assume there is a stuck at '0' fault at y. Since y was stuck at '0', it will give always '0' as the output. However when this value is passed to repairing circuit, it detects the fault and produces correct output. This is shown in Fig. 6. Similarly assume there is a stuck at '1' fault at y. Since y was stuck at '1', it will give always '1' as the output. However when this value is passed to repairing circuit, it detects the fault and produces correct output. This is shown in Fig. 7.

So when there is fault in multiplexer block, then output Op gives the inverted value of y. If there is no fault, then y value is passed to the output Op.

The above proposed multiplexer 1 uses additional circuitry to repair. In the proposed self repairing multiplexer 2 the building blocks of multiplexer itself are self repairable.

IV. PROPOSED SELF REPAIRING MULTIPLEXER 2

The building blocks of this type multiplexer are itself self repairing. The circuit diagram is shown in Fig. 3. In this circuit the logic blocks are self repairing and all the faults are both detectable and repairable. The self repairing structures of AND & OR gate are shown in Fig. 4 and Fig. 5 respectively.

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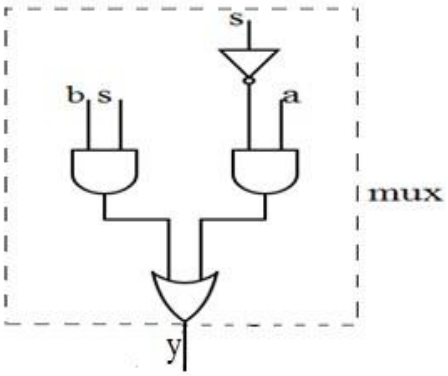

Fig. 3. Proposed self repairing multiplexer 2

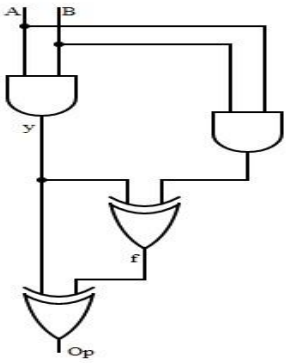

Fig. 4. Proposed self repairing AND gate

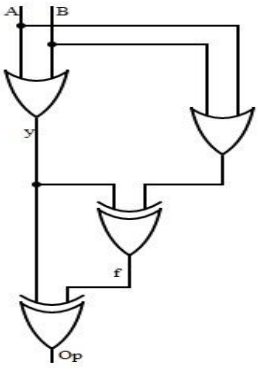

Fig. 5. Proposed self repairing OR gate

Consider Fig. 4. When there is fault in the AND gate which output is ‘y’, then f will become logic 1 and circuit gives output Op as inverted value of y. Similarly when there is no fault, then f will give logic 0 and the circuit output Op as the value of y.
Similarly consider Fig. 5. When there is fault in the OR gate output Op as inverted value of y. Similarly when there which output is ‘y’, then f will become logic 1 and circuit gives

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fig. 10. Result of proposed self repairing multiplexer 2 for fault free case

the value of y. Thus any fault can be self repairable by using the self repairing blocks.

V. SIMULATION RESULTS

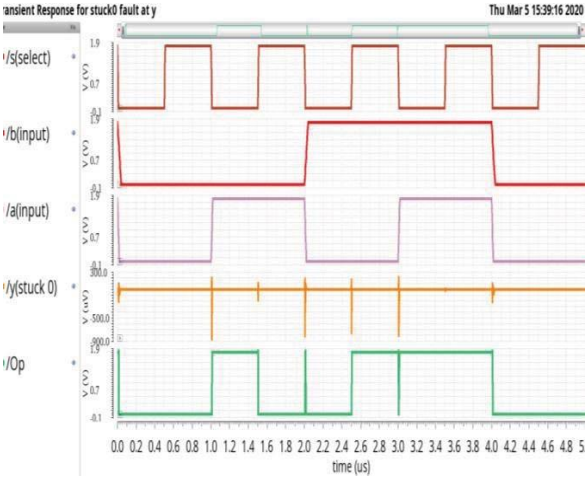

Fig. 6. Result of proposed self repairing multiplexer 1 for stuck fault

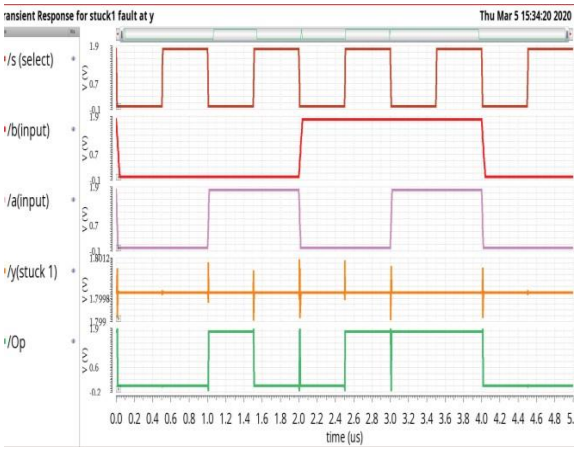

Fig. 7. Result of proposed self repairing multiplexer 1 for stuck fault

The simulation was done using cadence virtuoso tool using 180nm technology. The voltage of 1.8 V is used for power supply. The result is verified for all the combinations of inputs and all the possible stuck at faults. The proposed structures outputs are reported in Table I. Fig. 6 shows the result of proposed self-repairing multiplexer 1 for stuck '0' fault, Fig. 7 shows result of proposed self repairing multiplexer 1 for stuck '1' fault, Fig. 8 shows result of proposed self repairing multiplexer 1 for fault free case, Fig. 9 shows result of proposed self repairing multiplexer 2 for stuck at'1' fault in AND gate and Fig. 10 shows result of proposed self repairing multiplexer 2 for fault free case respectively.

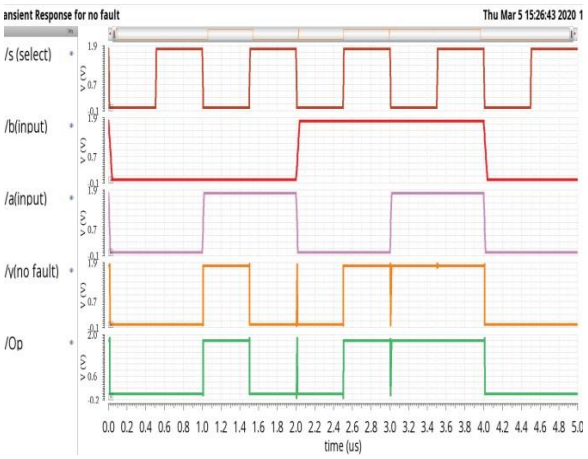

Fig. 8. Result of proposed self repairing multiplexer 1 for fault free case

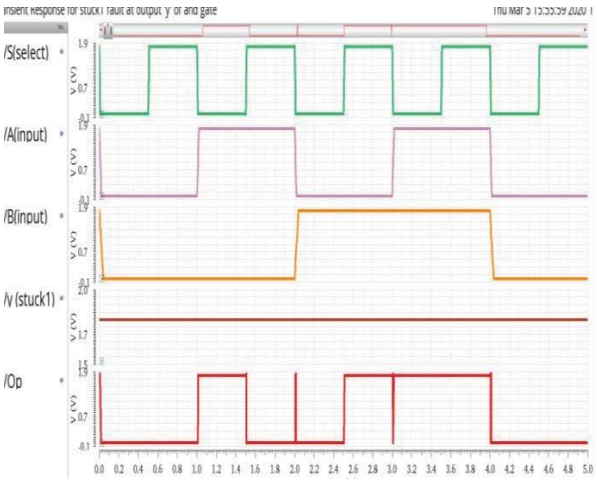

Fig. 9. Result of proposed self repairing multiplexer 2 for stuck fault in AND gate

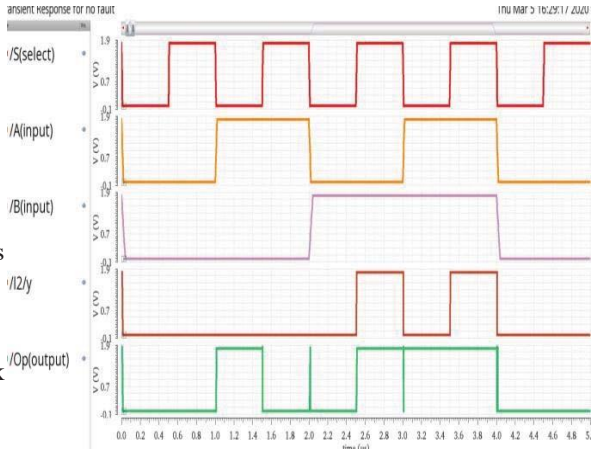

Table I

Power, delay and PDP values of the proposed structures.

Multiplexer	Proposed self repairing multiplexer 1	Proposed self repairing multiplexer 2
Power(μW)	90.92	111.5
Delay(n sec)	7.69	13.12
PDP	699.36	1462.88

VI. CONCLUSION

As the multiplexer is very vital component in many systems, faults in multiplexer lead to inaccurate results in the systems. Fault tolerant systems must need fault tolerant multiplexer to avoid faults. The proposed self repairing multiplexers can be used in multi bit adders, multipliers etc. The proposed self repairing multiplexers can be used in fault tolerant systems to get 100% error recoverability. The structure repairs itself so that no external inputs are required to repair. This avoids the area overhead. The circuits are simulated and verified the outputs. The fault tolerance of the proposed structures is verified.

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